CLMPTO

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1. (Currently Amended) A chip-scale package for photonic devices, comprising:

a window having one or more conductive traces on a first side of said window;

a chip fixed relative to the first side of said window, said chip having at least one electrical terminal;

a first housing having a body with an outer surface and an inner surface and extending around said chip and fixed relative to said window, said first housing having one or more electrical terminals along its outer surface that are electrically connected, through the body via an embedded trace in the housing, to at least one electrical terminal along the inner surface of the housing; and

~~said chip having one or more electrical terminals;~~

~~said first housing having one or more electrical terminals; and~~

at least one terminal of said chip being bump bonded to a first conductive trace on said window, and at least one said electrical terminal along the inner surface of the housing ~~least one terminal of said first housing~~ being bump bonded to said first [[a]] conductive trace on said window.

2. (Original) The package of claim 1, wherein said chip is hermetically sealed by said window and said first housing.

3. (Original) The package of claim 2, wherein said first housing is sealed to said window at the periphery of said window by a sealing-type material.

4. (Cancelled)

5. (Previously Presented) The package of claim 1, wherein said chip comprises a photonic device.

6. (Cancelled)

7. (Previously Presented) The package of claim 5, further comprising a second housing situated adjacent to a second side of said window.

8. (Withdrawn) The package of claim 7, further comprising a ferrule having at least one optical fiber, which is placed adjacent said second side of said window.

9. (Withdrawn) The package of claim 8, further comprising a lens formed on or in said window.

10. (Withdrawn) The package of claim 9, wherein said ferrule is accepted by an opening in said second housing.

11. (Withdrawn) The package of claim 10, wherein an end of said optical fiber is proximate to said window so that light from the fiber can go through the optical fiber and said window to the photonic device, and/or so that light from the photonic device can go through said window and the least one optical fiber.

12-32. (Cancelled)

33. (Currently Amended) A chip-scale package for electronic devices, comprising:

a transparent window having at least one conductive trace patterned on a surface of said window;

a semiconductor chip fixed relative to said window having at least one terminal connected to the at least one conductive trace;

a first housing surrounding said chip and affixed to said window; and

a conductive path embedded in said housing from the at least one conductive trace to an at least one pad on an external surface of said housing ~~enclosure~~.

34. (Original) The package of claim 33, wherein said chip comprises a photonic device.

35. (Original) The package of claim 34, wherein said window has at least one feature on the surface of said window for alignment.

36. (Cancelled)

Cancelled claims 37-47

48. (Original) The package of claim 35, further comprising a second housing attached to said first housing.

49. (Original) The package of claim 48, wherein said second housing is mechanically registered to said first housing by the at least one feature on the surface of said window.

50. (Withdrawn) The package of claim 49, further comprising a ferrule having at least one optical waveguide.

51. (Withdrawn) The package of claim 50, wherein the at least one optical waveguide is proximate to said window so that light from the waveguide can pass through said window to the at least one photonic device, and/or so that light from the photonic device can go through said window and to the at least one optical waveguide.

52. (Withdrawn) The package of claim 51, wherein said window has at least one lens situated between the at least one photonic device and said at least one optical waveguide.

53. (Withdrawn) The package of claim 52, wherein the at least one optical waveguide is an optical fiber.

54. (Withdrawn) The package of claim 51, further comprising at least one pin securing said ferrule to said first housing.

55. (Original) The package of claim 34, wherein the at least one photonic device is a VCSEL.

56. (Original) The package of claim 33, wherein said first housing comprises ceramic.

57. (Original) The package of claim 33, wherein said window comprises quartz.

58. (Previously Presented) The package of claim 1, wherein the at least one terminal of said chip is bump bonded to the same conductive trace as the at least one terminal of said first housing.

59. (Previously Presented) The package of claim 1, wherein the at least one terminal of said first housing is electrically connected to a terminal outside of said first housing.

60. (Previously Presented) The package of claim 59, wherein said first housing is a multi-layer housing, and the at least one terminal of said first housing is electrically connected to a terminal outside of said first housing via a trace in the multi-layer housing.

61. (Previously Presented) The package of claim 60, wherein said chip includes a back side facing away from said window, wherein the back side of said chip is electrically connected to a terminal outside of said first housing via another trace in the multi-layer housing.

62. (Previously Presented) A chip-scale package for photonic devices, comprising:

a window;

a chip fixed relative to a first side of said window;

a first housing having a body with an outer surface and an inner surface, the inner surface extending around said chip and fixed relative to said window to form a chip cavity;

said first housing having at least one electrical terminal along its outer surface, which is electrically connected by an embedded electrical path through the body of the first housing to at least one electrical terminal along the inner surface of the first housing;

said window includes one or more conductive traces;

said chip includes one or more electrical terminals; and

at least one terminal of said chip is bump bonded to a conductive trace on said window, and at least one terminal along the inner surface of the first housing is bump bonded to a conductive trace on said window.

63. (Cancelled)

64. (Previously Presented) The package of claim 62, wherein the at least one terminal of said chip is bump bonded to the same conductive trace as the at least one terminal of said first housing.

65. (Previously Presented) The package of claim 62, wherein said first housing is a multi-layer housing.

66. – 68. (Cancelled)

69. (New) A chip-scale package for photonic devices, comprising:

a first housing having a body, an electrically conductive internal pad, an electrical path connected to said internal pad and embedded in said body, and an electrically conductive external pad connected to said electrical path;

a chip attached relative to said first housing, the chip having an electrically conductive pad that faces the window; and

a window attached relative to said first housing, wherein the internal pad of the housing faces said window;

at least one conductive trace formed on said window; and

wherein the at least one conductive trace is electrically connected to the pad of said chip and to the internal pad of said first housing.

70. (New) The package of claim 69, wherein said first housing and said window form a hermetically sealed volume containing said chip.

71. (New) The package of claim 70, wherein the first housing further includes an external pad situated externally relative to the sealed volume which is electrically connected to the internal pad of the first housing.

72. (New) The package of claim 71, further comprising a second housing attached to said first housing.

73. (New) The package of claim 72, wherein said chip has at least one photonic device.

74. (New) A hermetic chip-scale package comprising:

a first housing;

an integrated circuit mounted within said first housing, the integrated circuit having at least one terminal;

a window secured relative to said first housing; and

wherein:

said integrated circuit has at least one photonic device; and

said first housing and said window form a hermetically sealed enclosure around said integrated circuit, said housing having a body with at least one conductor extending on an embedded path from an inner surface of the housing at the hermetically sealed enclosure to an outer surface of the housing, the at least one conductor having a low resistance path to a terminal of the integrated circuit.

75. (New) The package of claim 74, wherein said window comprises at least one conductive trace connected to said terminal of said integrated circuit.

76. (New) The package of claim 75, wherein the conductor of said housing is connected to the at least one conductive trace, for providing a connection from the at least one conductive trace external to the hermetically sealed enclosure.

77. (New) The package of claim 76, further comprising a second housing situated adjacent to said window, wherein said second housing has at least one alignment feature.

78. (New) A chip-scale package for photonic devices, comprising:

a window;

a chip fixed relative to a first side of said window;

a housing having a body with an outer surface and an inner surface, the inner surface extending around said chip and fixed relative to said window to form a chip cavity; and

said housing being monolithic and having at least one electrical terminal along its outer surface, which is electrically connected through the body via an embedded trace in the housing to at least one electrical terminal along the inner surface of the housing.

79. (New) The package of claim 78 wherein the window and the housing form a hermetically sealed chip cavity.

80. (New) A chip-scale package for photonic devices, comprising:

a window;

a chip fixed relative to a first side of said window;

a housing having a body with an outer surface and an inner surface, the inner surface extending around at least part of said chip and fixed relative to said window to form a hermetically sealed chip cavity;

said housing having at least one electrical terminal along its outer surface, which is electrically connected through an embedded path in the body of the housing to at least one electrical terminal along the inner surface of the housing.